

FIGURE 1

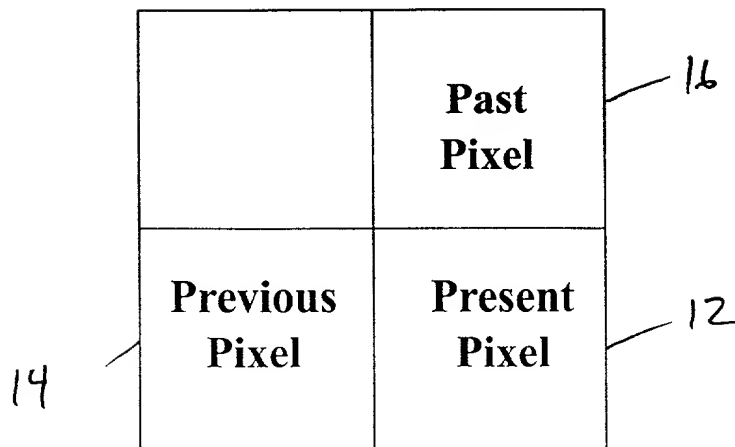


FIGURE 2

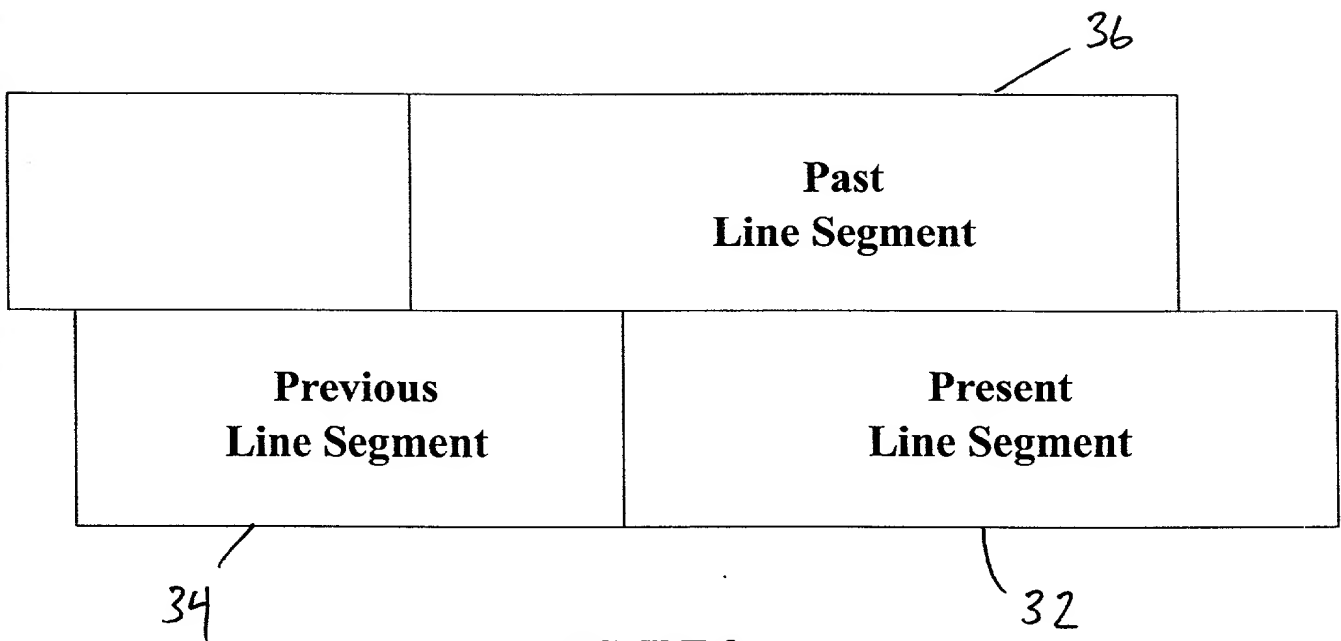
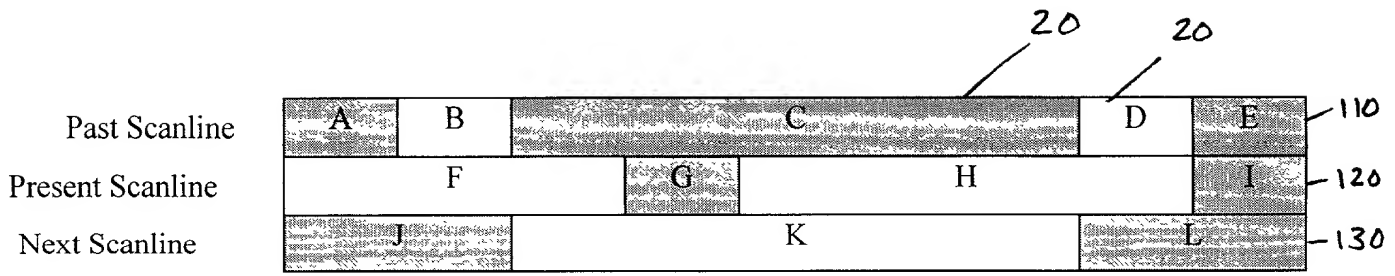


FIGURE 3



100 ↗

FIGURE 4

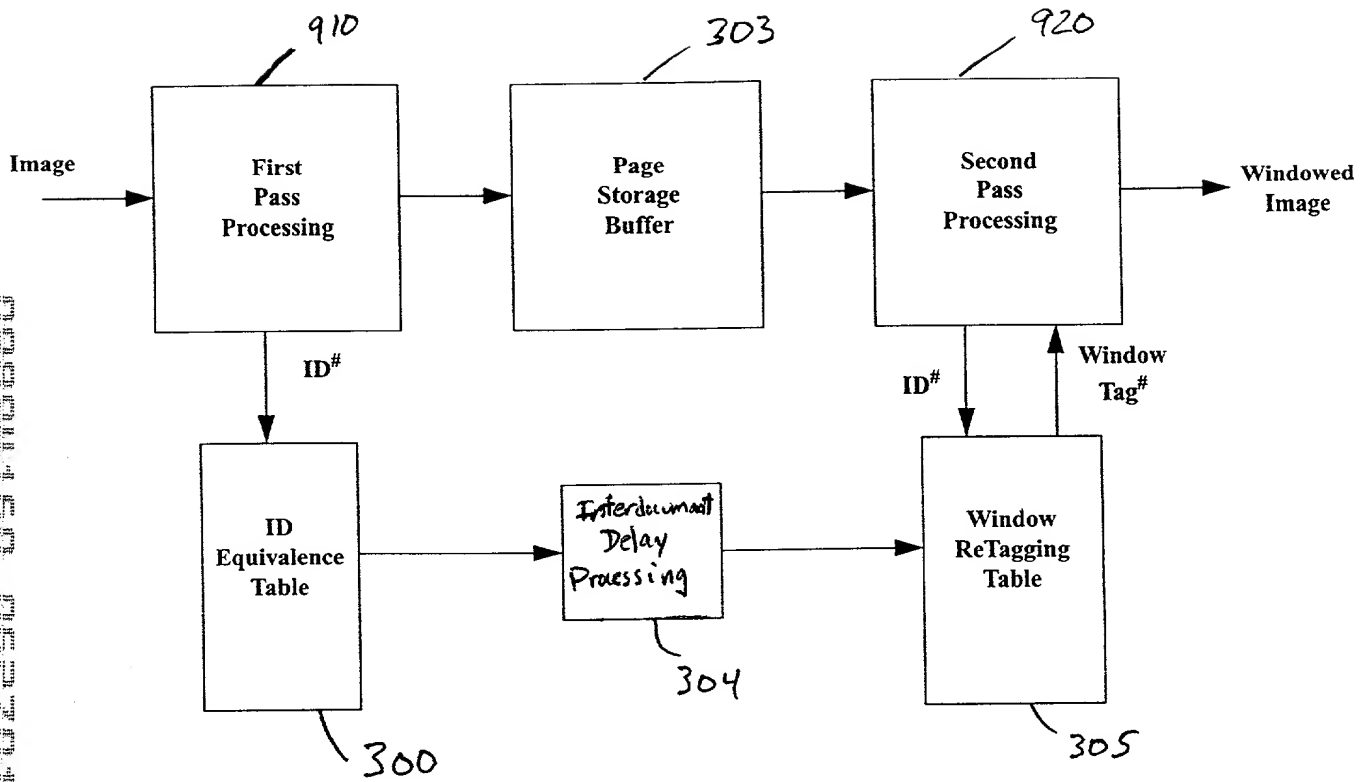


FIGURE 5

912

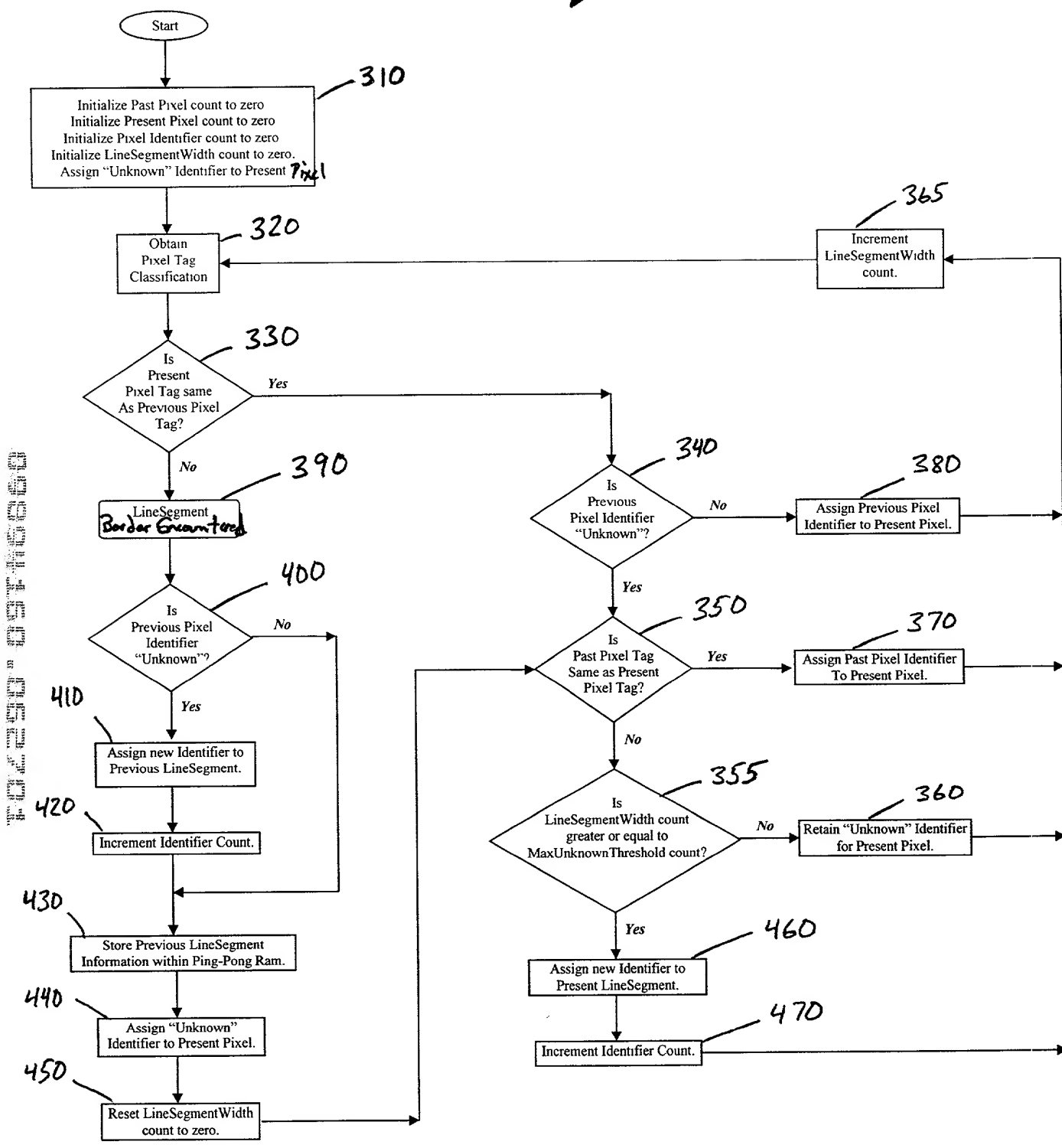


FIGURE 6

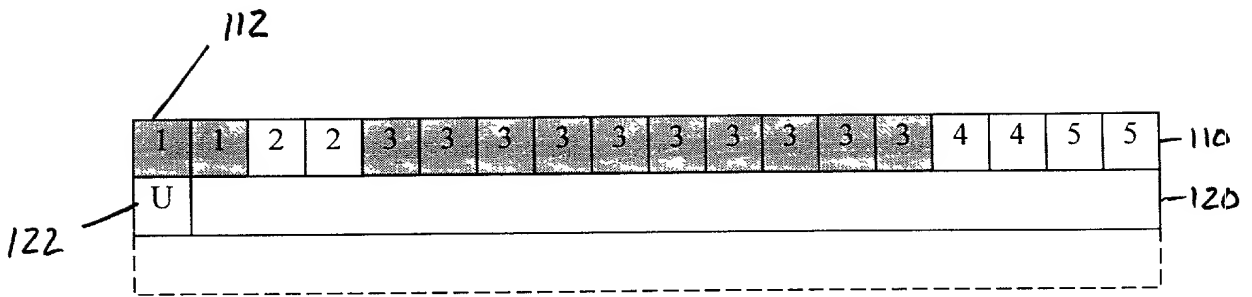


FIGURE 7A

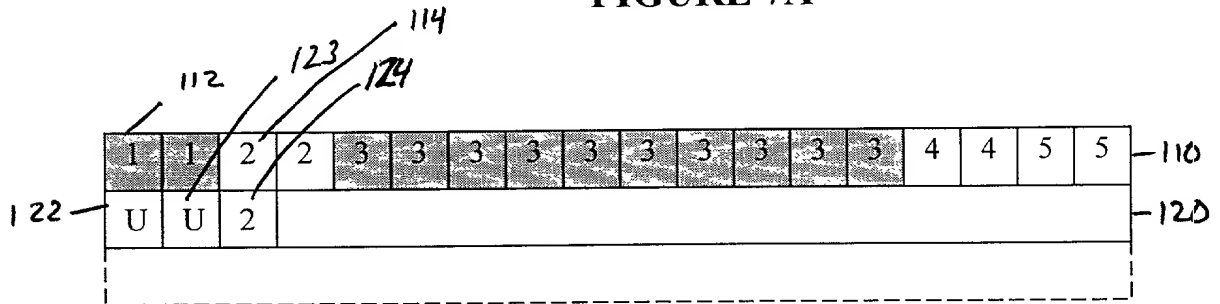


FIGURE 7B

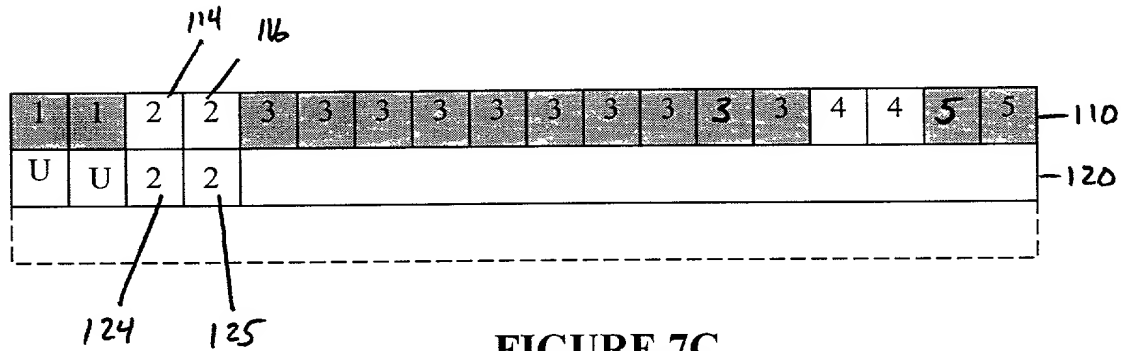


FIGURE 7C

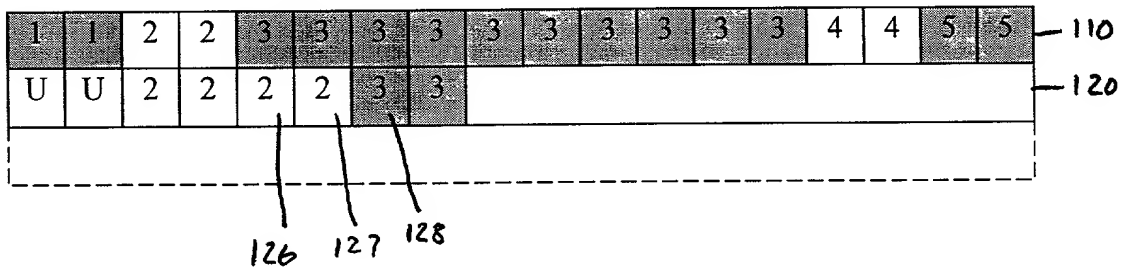


FIGURE 7D

1	1	2	2	3	3	3	3	3	3	3	3	3	3	4	4	5	5	110
U	U	2	2	2	2	3	3	U	U	U	U	U	U	6				120
																		129

FIGURE 7E

1	1	2	2	3	3	3	3	3	3	3	3	3	3	4	4	5	5	110
U	U	2	2	2	2	3	3	U	U	U	U	U	6	6	6	5	5	120
																		129

FIGURE 7F

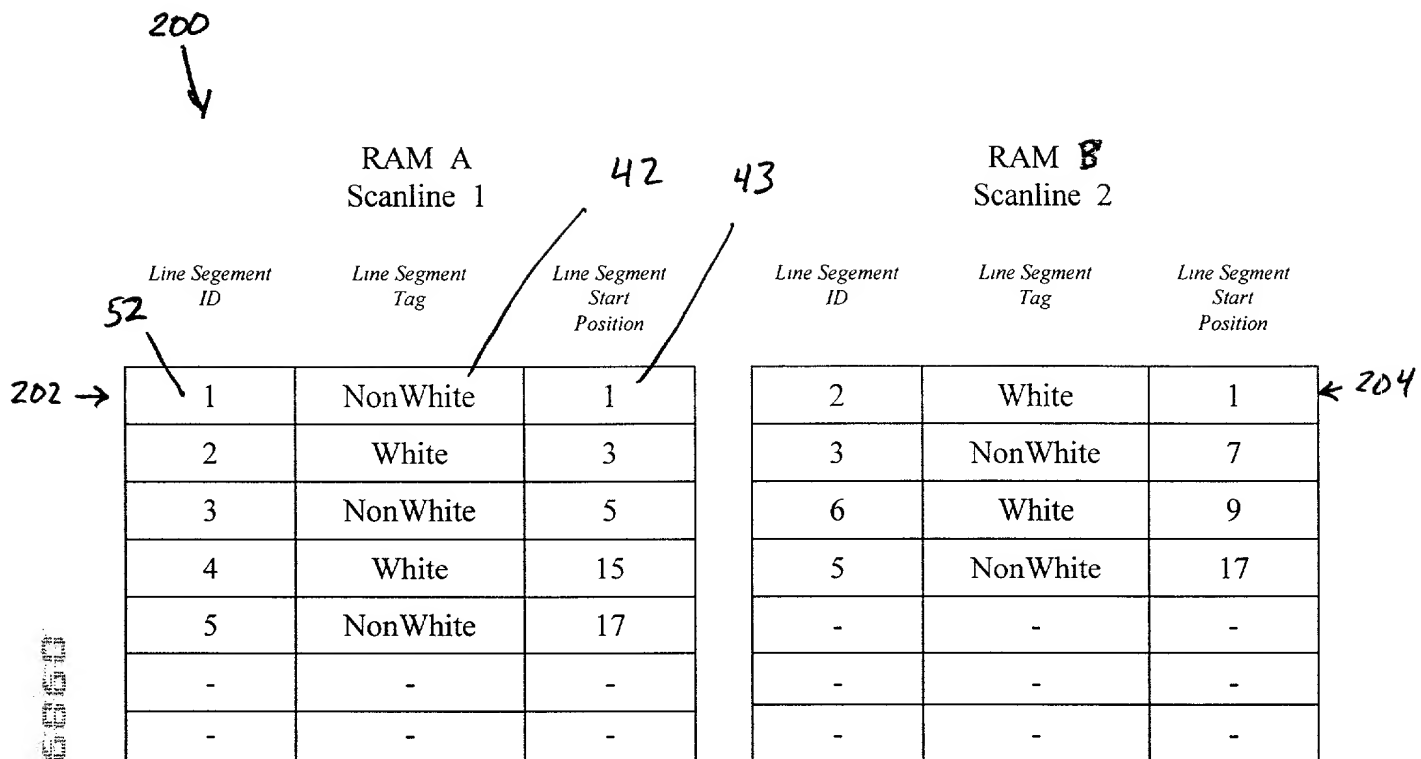


FIGURE 8

300
↓

Address

Entry

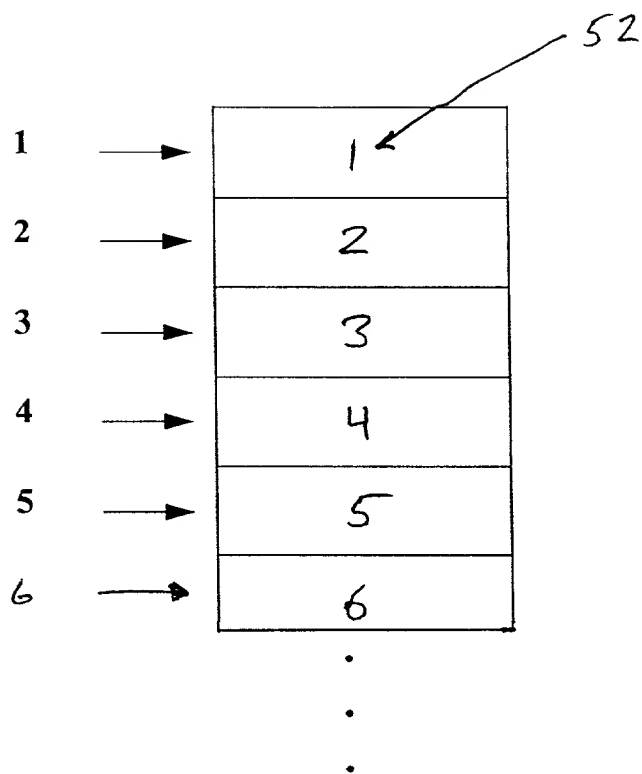


FIGURE 9

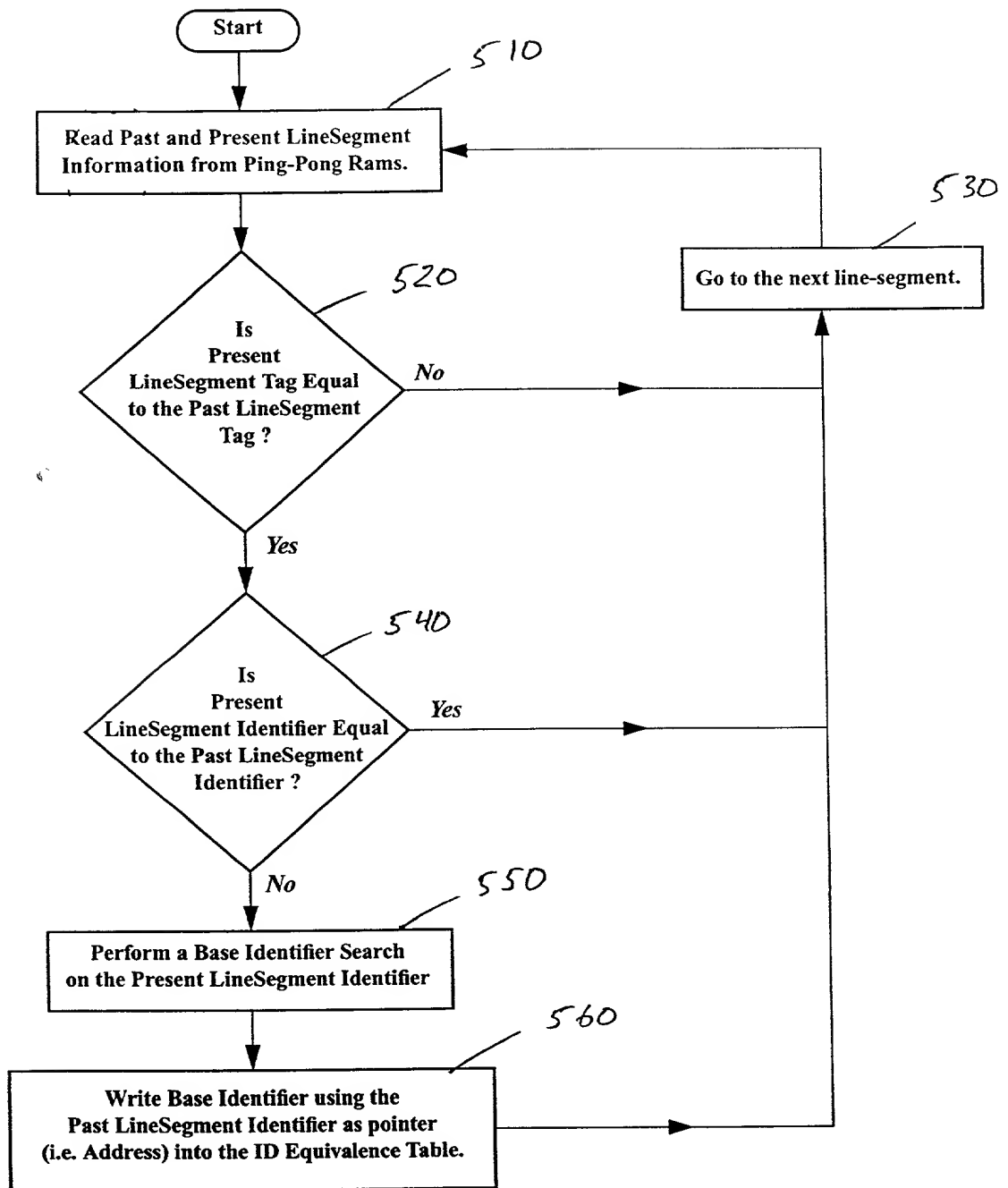


FIGURE 10

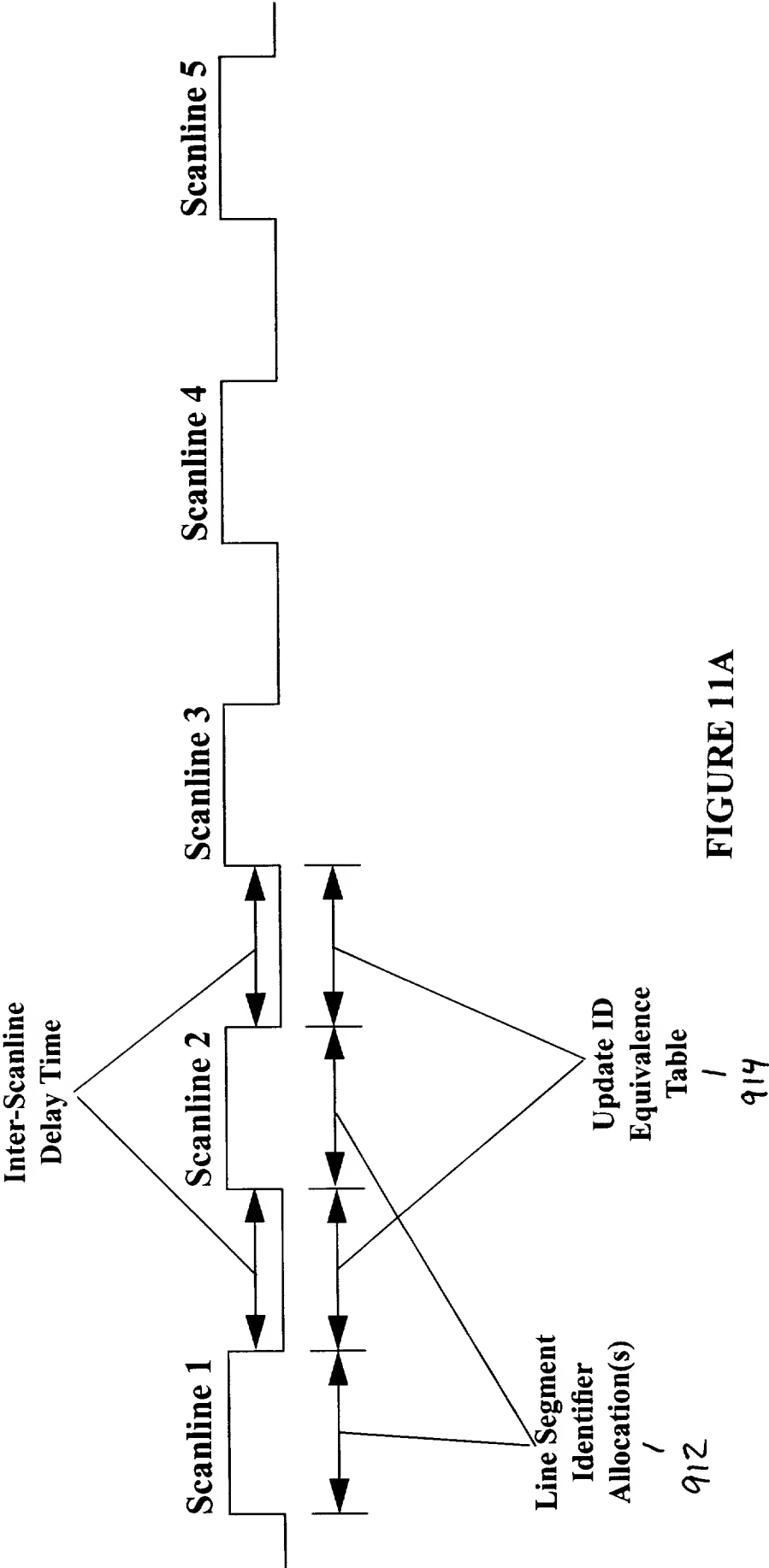


FIGURE 11A

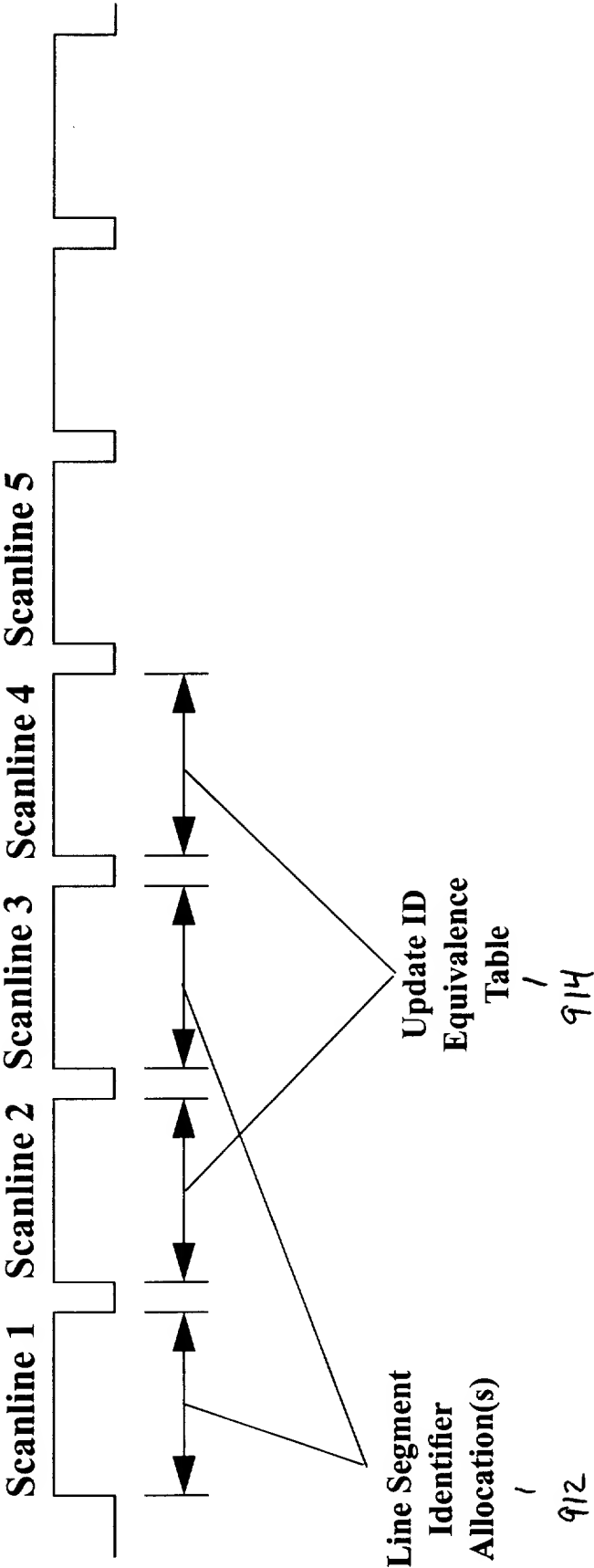


FIGURE 11B

Address	Entry
1	1
2	2
3	3
4	6
5	5
6	6
7	7
-	-

300 ↗

FIGURE 12

1	1	2	2	3	3	3	3	3	3	3	3	3	3	4	4	5	5	110
U	U	2	2	2	2	3	3	U	U	U	U	U	6	6	6	5	5	120
U	U	U	U	2	2	2	2	2	2	2	2	2	2	U	U	5	5	130

FIGURE 13A

100 ↗

FIG. 13A

200
↓

RAM A
Scanline 3

RAM B
Scanline 2

	<i>Line Segment ID</i>	<i>Line Segment Tag</i>	<i>Line Segment Start Position</i>		<i>Line Segment ID</i>	<i>Line Segment Tag</i>	<i>Line Segment Start Position</i>	
202 →	7	NonWhite	1		2	White	1	← 204
206 →	2	White	5		3	NonWhite	7	← 208
210 →	5	NonWhite	15		6	White	9	← 212
	-	-	-		5	NonWhite	17	← 216
	-	-	-		-	-	-	
	-	-	-		-	-	-	
	-	-	-		-	-	-	
	-	-	-		-	-	-	

FIGURE 14

Address	Entry
1	1
2	2
3	3
4	6
5	5
6	2
7	7
-	-

300 →

FIGURE 15

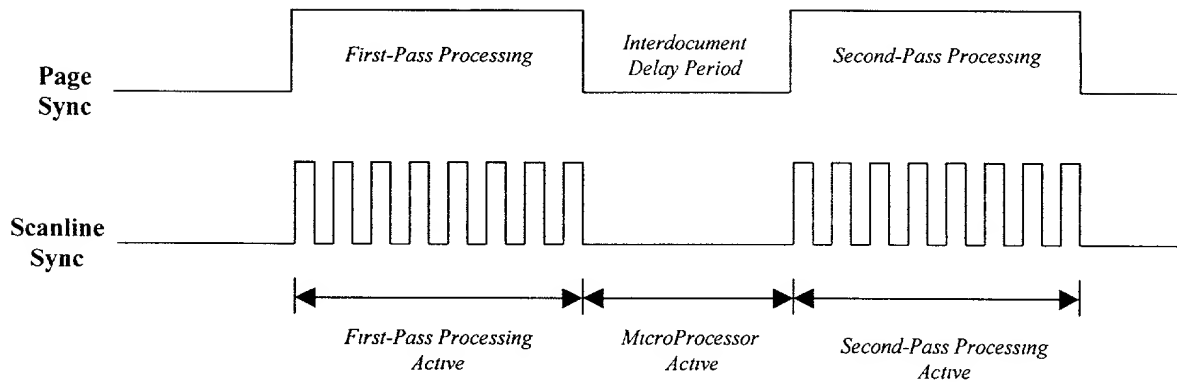


FIGURE 16

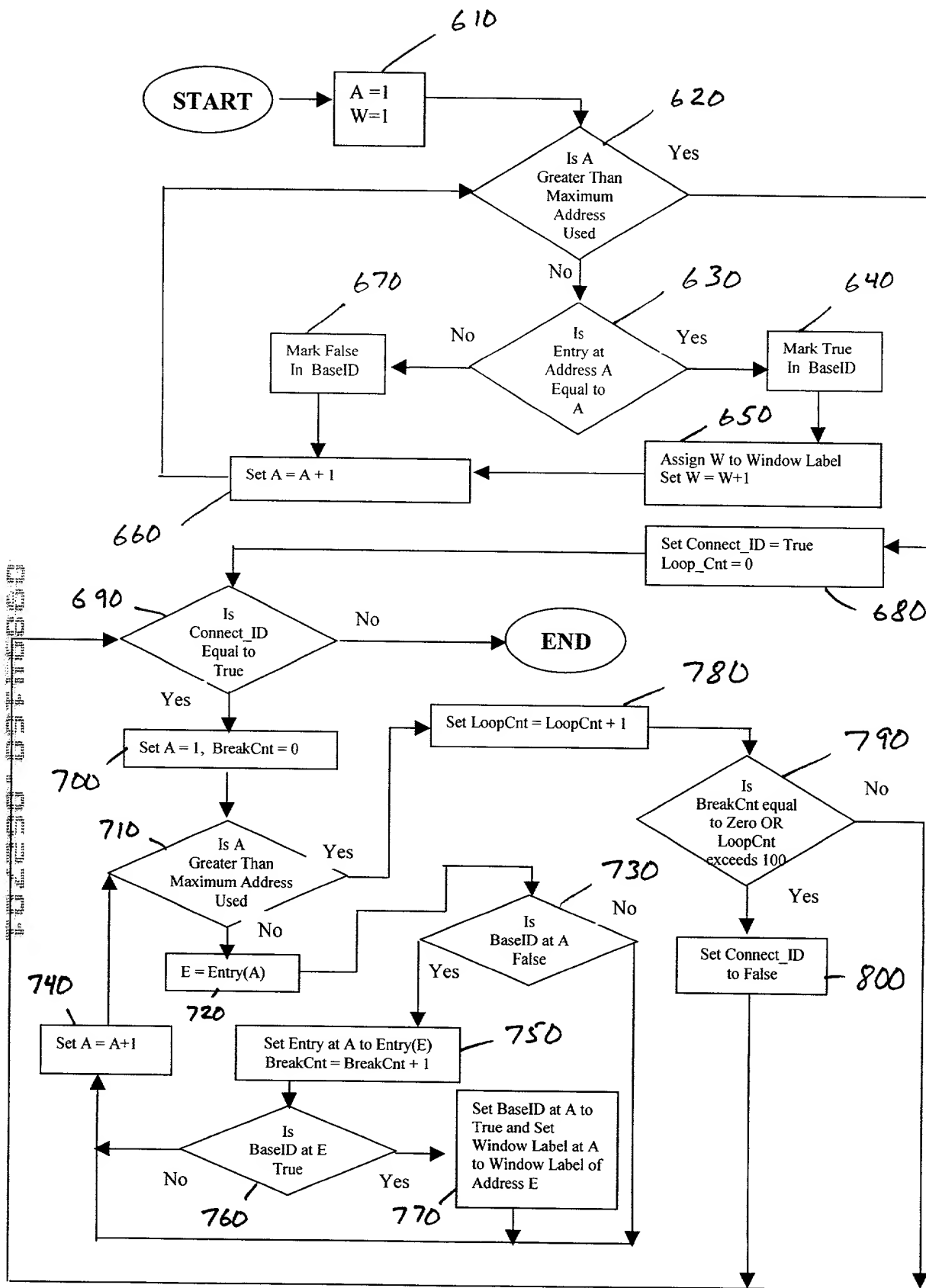


FIGURE 17

FIGURE 18A

302 →

Address	Entry ³⁰⁷	BaseID ³⁰⁸	Window ³⁰⁹
1	1	True	W1
2	2	True	W2
3	3	True	W3
4	6	False	
5	5	True	W4
6	2	False	
7	7	True	W5
-	-	-	-

FIGURE 18B

302 →

Address	Entry ³⁰⁷	BaseID ³⁰⁸	Window ³⁰⁹
1	1	True	W1
2	2	True	W2
3	3	True	W3
4	2	False	
5	5	True	W4
6	2	True	W2
7	7	True	W5
-	-	-	-

FIGURE 18C

302 →

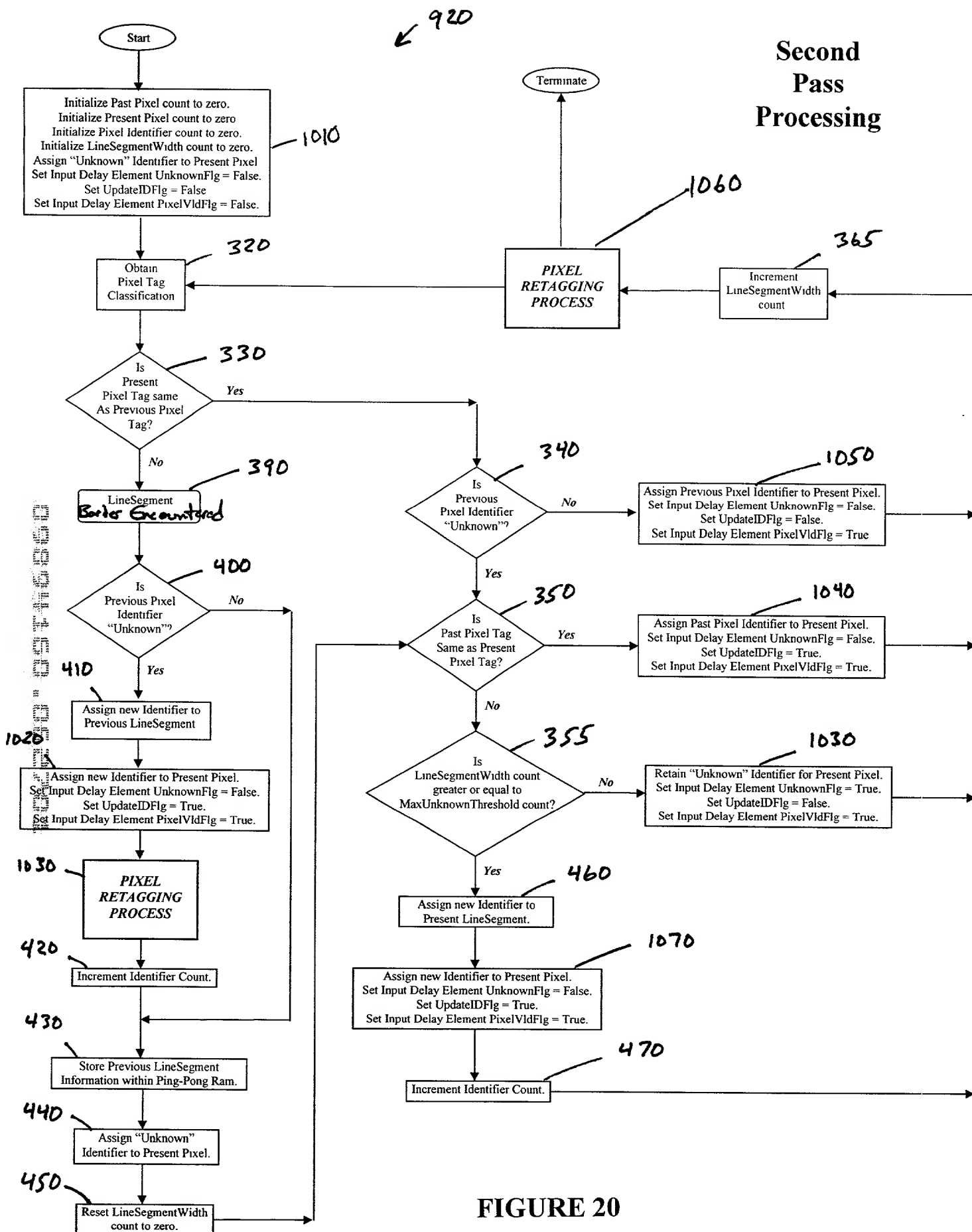
Address	Entry ³⁰⁷	BaseID ³⁰⁸	Window ³⁰⁹
1	1	True	W1
2	2	True	W2
3	3	True	W3
4	2	True	W2
5	5	True	W4
6	2	True	W2
7	7	True	W5
-	-	-	-

309
↓

Address	Window Label
1	W1
2	W2
3	W3
4	W2
5	W4
6	W2
7	W5
-	-

305 ↗

FIGURE 19



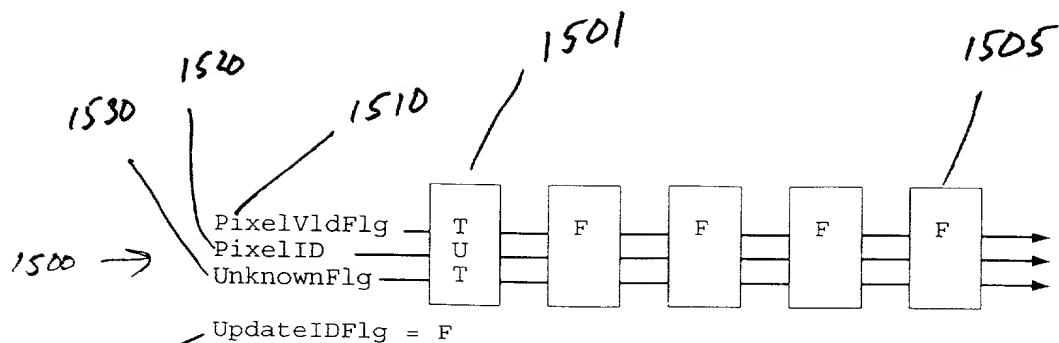


FIGURE 21A

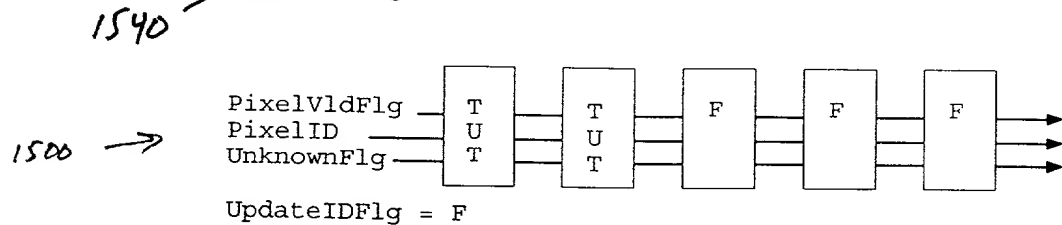


FIGURE 21B

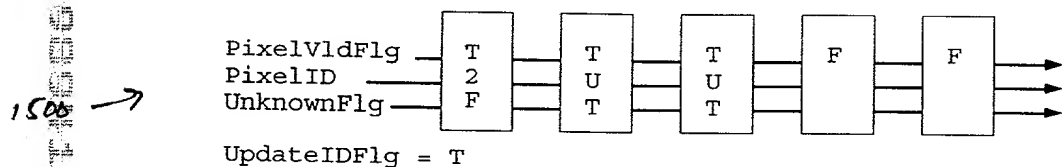


FIGURE 21C

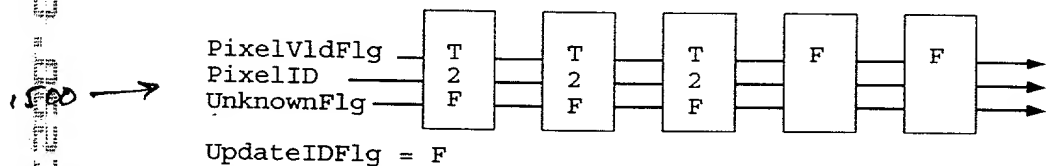


FIGURE 21D

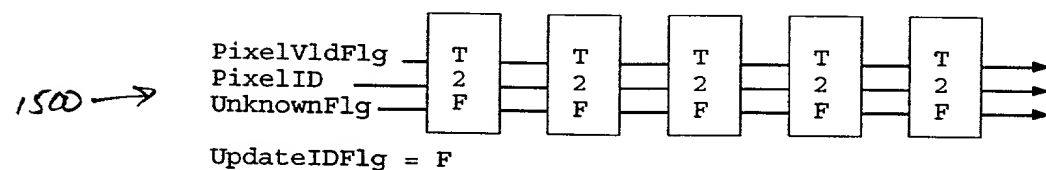


FIGURE 21E

PIXEL RETAGGING PROCESS

922 →

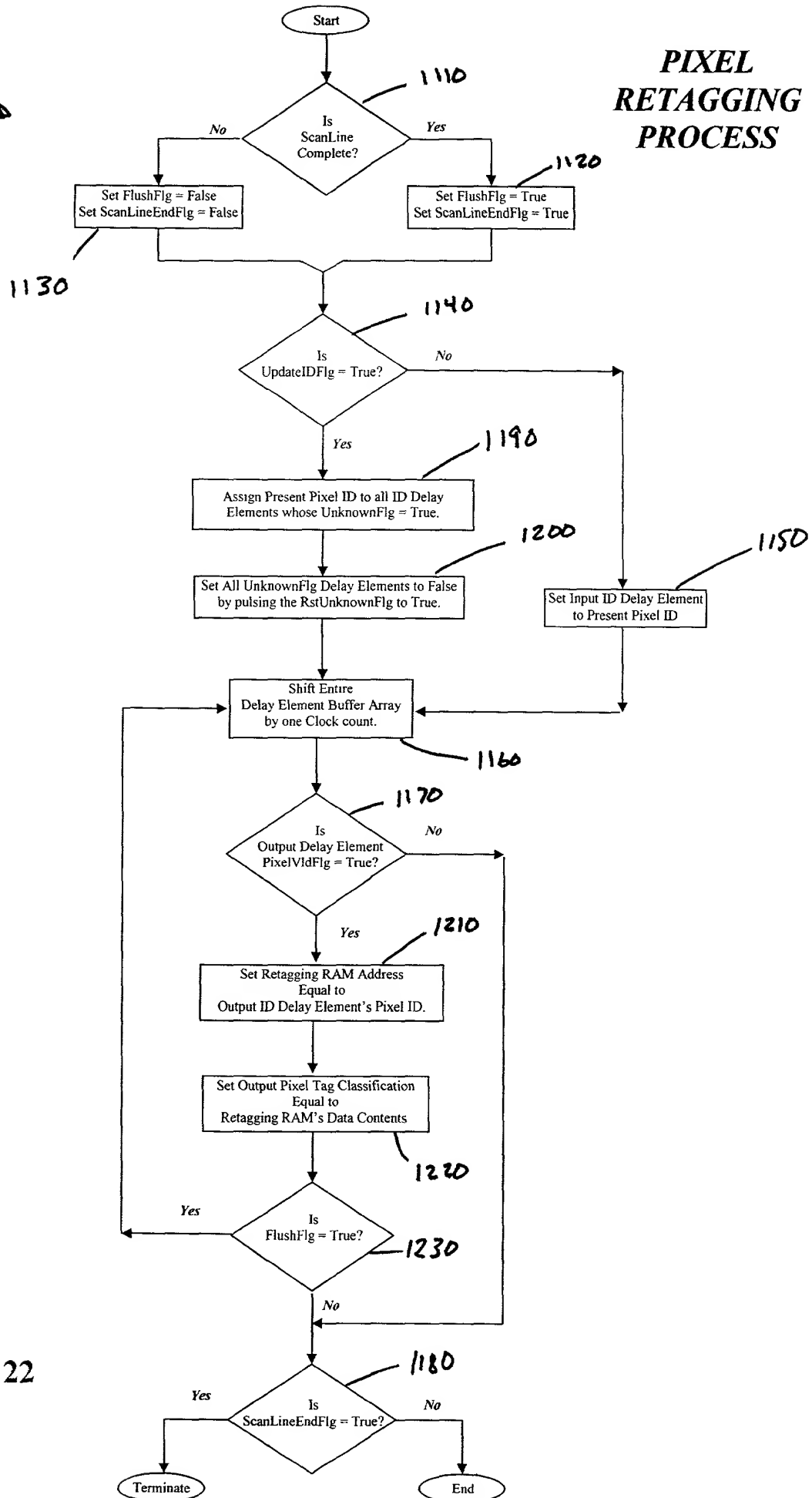


FIGURE 22

W1	W2	W3	W2	W4
W2		W3	W2	W4
W5	W2			W4

100 ↗

FIGURE 23

FIG. 23 is a schematic diagram of a system 100.

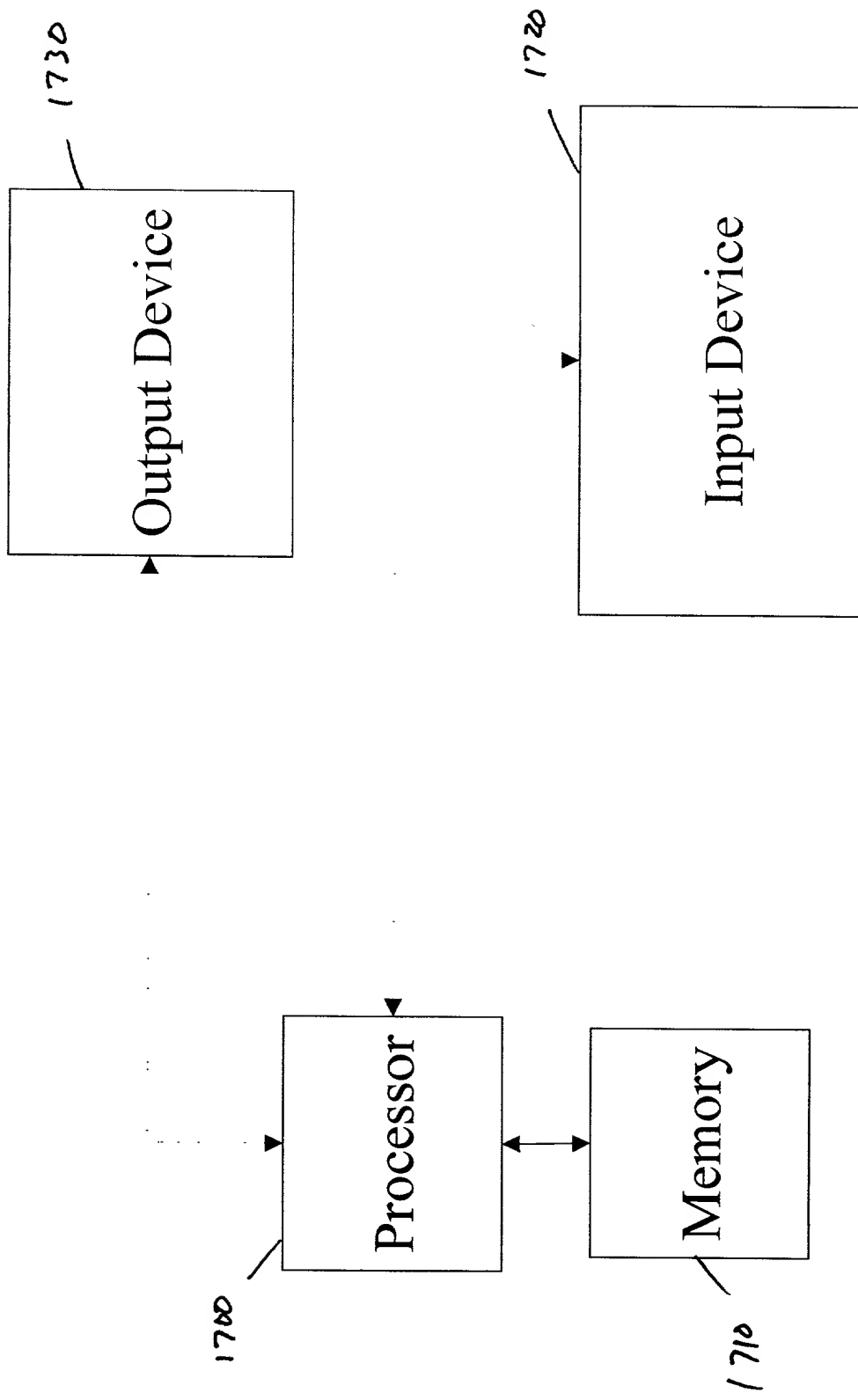


FIGURE 24